

What is claimed is:

1 1. A method for increasing the capacitance of deep
2 trench capacitors, comprising:
3 providing a substrate;
4 forming a pad structure on the substrate;
5 forming a patterned photoresist layer on the pad
6 structure, wherein a trench region is defined
7 by the region uncovered by the patterned
8 photoresist layer;
9 forming a trench in the substrate using the
10 patterned photoresist layer and the pad
11 structure as an etching mask;
12 removing the patterned photoresist layer;
13 forming a trench capacitor in the lower portion of
14 the trench;
15 forming a first insulation layer on the trench
16 capacitor;
17 forming an epitaxy layer on the sidewalls of the
18 trench above the first insulation layer as a
19 liner to narrow the dimension of the trench;
20 and
21 removing the first insulation layer uncovered by the
22 epitaxy layer.

1 2. The method as claimed in claim 1, wherein the
2 substrate is made of P-type silicon, N-type silicon, or
3 non-doped epitaxy silicon.

1 3. The method as claimed in claim 1, wherein the
2 first insulation layer is made of high density plasma
3 oxide silicon.

1 4. The method as claimed in claim 1, wherein the
2 epitaxy layer is made of P-type epitaxy silicon, N-type
3 epitaxy silicon, or non-doped epitaxy silicon.

1 5. The method as claimed in claim 1, wherein the
2 thickness of the epitaxy layer is 100~200 Å.

1 6. The method as claimed in claim 1, wherein the
2 insulation layer uncovered by the epitaxy layer is
3 removed by wet etching.

1 7. A method for increasing the capacitance of deep
2 trench capacitors, comprising:

3 providing a substrate;

4 forming a pad structure on the substrate, wherein
5 the pad structure comprises a pad oxide layer
6 and a pad nitride silicon layer;

7 forming a patterned photoresist layer on the pad
8 structure, wherein a trench region is defined
9 by the region uncovered by the patterned
10 photoresist layer, and the dimension of the
11 region exceeds a predetermined dimension of the
12 trench region;

13 etching the pad structure uncovered by the patterned
14 photoresist layer using the patterned
15 photoresist layer as a mask;

16 etching the substrate uncovered by the pad structure
17 using the patterned photoresist layer and the
18 pad structure as a mask, thereby forming a
19 trench in the substrate;
20 removing the patterned photoresist layer;
21 forming a trench capacitor in the lower portion of
22 the trench, wherein the trench capacitor
23 comprises a buried electrode plate, a capacitor
24 dielectric layer, and a first conductive layer,
25 as another electrode plate of the trench
26 capacitor;
27 forming a first insulation layer on the trench
28 capacitor, the sidewalls of the trench, and the
29 pad structure;
30 removing the first insulation layer covering the
31 sidewalls of the trench and the pad structure
32 by etching, thus forming the first insulation
33 layer on the trench capacitor;
34 forming an epitaxy layer on the pad structure, the
35 first insulation layer, and the sidewalls of
36 the trench;
37 removing the epitaxy layer on the pad structure and
38 the first insulation layer by etching, thus
39 forming an epitaxy layer on the sidewalls of
40 the trench as a liner to narrow the dimension
41 of the trench; and
42 removing the first insulation layer uncovered by the
43 epitaxy layer.

1 8. The method as claimed in claim 7, wherein the
2 substrate is made of P-type silicon, N-type silicon, or
3 non-doped epitaxy silicon.

1 9. The method as claimed in claim 7, wherein the
2 pad oxide layer of the pad structure is formed by thermal
3 oxidation.

1 10. The method as claimed in claim 7, wherein the
2 pad nitride silicon layer of the pad structure is formed
3 by chemical vapor deposition (CVD).

1 11. The method as claimed in claim 7, wherein the
2 buried electrode plate of the trench capacitor is an N-
3 type doped area.

1 12. The method as claimed in claim 7, wherein the
2 capacitor dielectric layer of the trench capacitor is
3 made of a stack layer comprising oxide-nitride (ON) or
4 oxide-nitride-oxide (ONO) silicon.

1 13. The method as claimed in claim 7, wherein the
2 first conductive layer of the trench capacitor is made of
3 doped polycrystalline silicon or doped non-
4 polycrystalline silicon.

1 14. The method as claimed in claim 7, wherein the
2 first insulation layer is made of high density plasma
3 oxide silicon.

1 15. The method as claimed in claim 7, wherein the
2 epitaxy layer is made of P-type epitaxy silicon, N-type
3 epitaxy silicon, or non-doped epitaxy silicon.

1 16. The method as claimed in claim 7, wherein the
2 thickness of the epitaxy layer is 100~200 Å.

1 17. The method as claimed in claim 7, wherein the
2 insulation layer uncovered by the epitaxy layer is
3 removed by wet etching.